**REPORT**

*Source Voltage Impact on CMOS Body Biasing*

FinFETs do not have an effectual “body”, making body biasing an ineffective method for influencing frequency and power consumption. Thus, we are interested in alternate methods for impacting the above variables in integrated circuits (ICs). Specifically, in this project, we will determine the impact of the source voltage on CMOS body biasing. We will do this by adjusting the source voltages for, first, a simple two-inverter setup and then ring oscillators of different sizes. It is important to note that our ring oscillators are constructed using two inverters for each gate rather than one. In a single two-inverter setup, we bias the top inverter with a +Vbias and the bottom inverter with a –Vbias. This is the design within each inverter in the ring oscillators, as well.

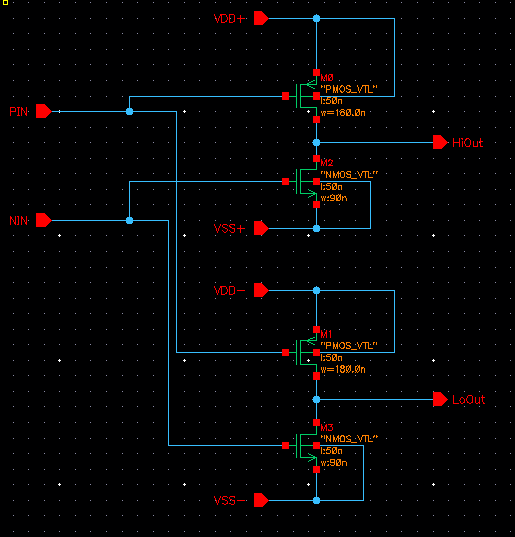
We, thus far, completed a variety of simulations, for which figures are attached. These simulations include:

* A design incorporating standard body-biasing to evaluate the effects.
* Our design (using varying supply voltages) compared to the effects of body biasing.
* Simple power analyses between our new two-inverter gate and a standard inverter with an equivalent logical effort.
* The transient (time-dependent) response of our new two-inverter gate in a ring oscillator.

For more information on these simulations, please see the attached figures. Prior to the proposal, we also plan to compare dynamic and static power consumption as we increase the bias voltage in an additional simulation.

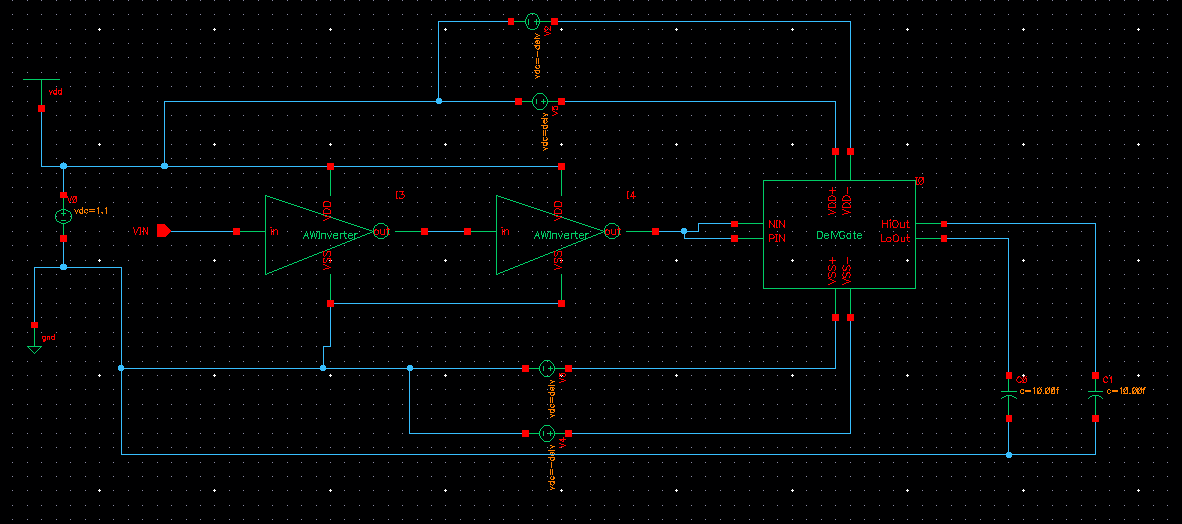
Following our proposal we will quantify increases in frequency and power consumption as compared to bias voltage. If our design proves to increase frequency without making sacrifices in power consumption, we will discuss applications.

SIMULATIONS



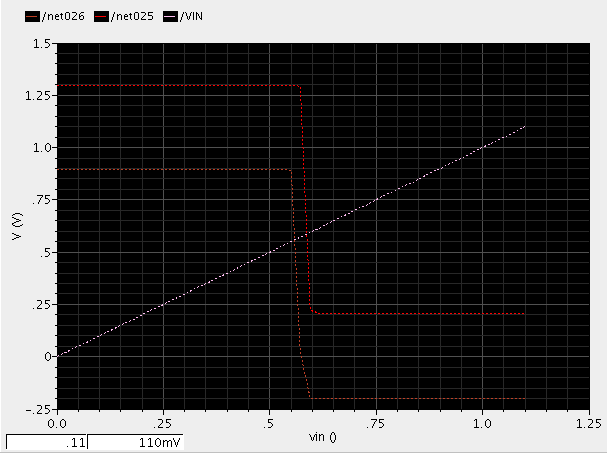
**Figure 1a: Schematic View of 2-Inverter Gate**

Notice in Figure 1a the four pins labeled VDD + & - and VSS+ & -. These are the conventions we will use to denote which inverter will have its source voltage shifted up (resulting in a strong high and weak low output) and which will be shifted down (resulting in strong low and weak high output). Note that the bulks for each device are tied to their sources to ensure that there is no body biasing effect in our analysis.



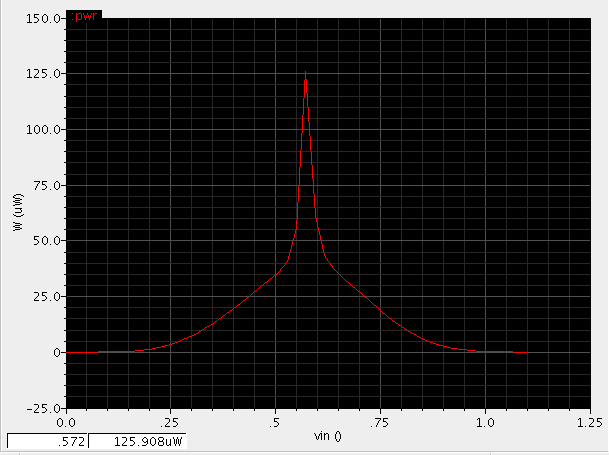
**Figure 1b: Test Bench for 2-Inverter Gate (denoted DelVGate)**

We ran the input through a buffer of two inverters before the signal was applied to our DelVGate.



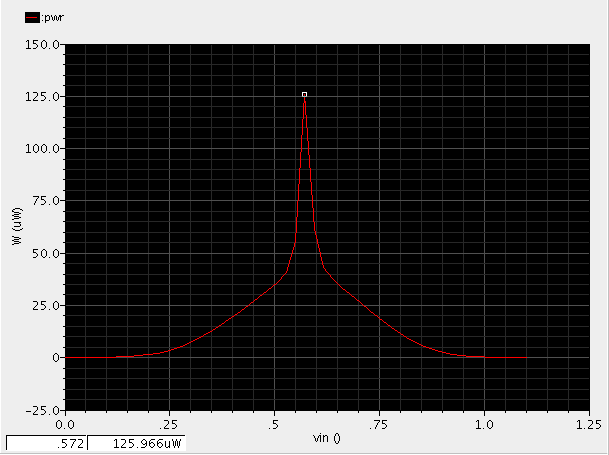
**Figure 1c: High and Low Output for 0-1.1 V DC Swept Input (VBIAS = 200 mV)**

We used a relatively large bias voltage to show a sharp contrast between the low and high outputs. The reason for the sharp curves is the low load capacitance used during the analysis (10f F for each output). This graph shows that on a high-low transition, the low output reaches its switching threshold faster that the high output, as expected.



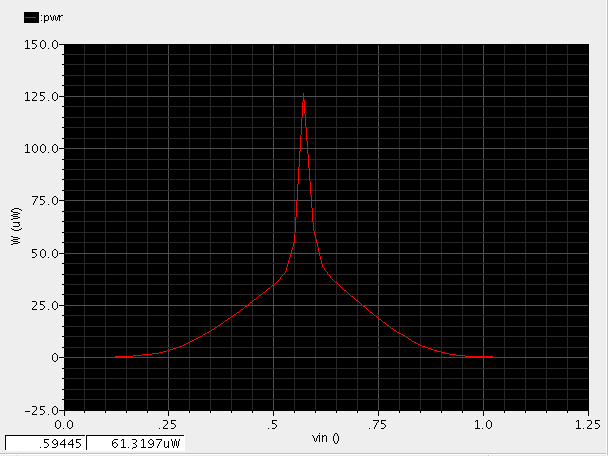
**Figure 1d: Total Power Consumption for High-to-Low Transition of 2-Inverter Gate Where VBias = 0**

Figure 1d shows the total power consumption for the test bench shown in figure 1b when the bias voltage is zero. This will be the base power analysis that we will test against in the following simulations. Note that this is not the power consumption of only our DelVGate, but also of the two buffer inverters. Hence, we will only make observations as to how the power consumption changes with VBIAS, and not draw quantitative results from the following analyses.



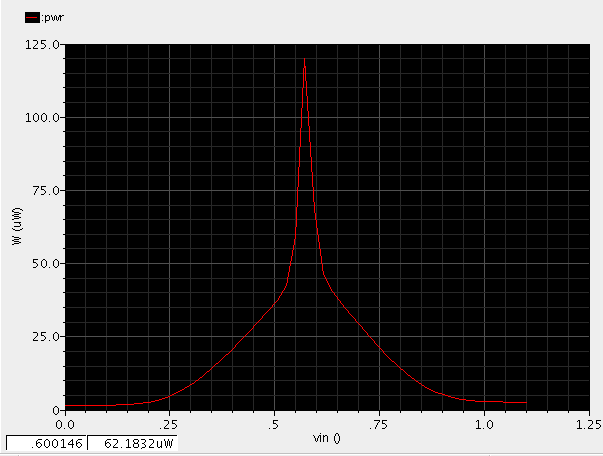
**Figure 1e: Total Power Consumption for Low-to-High Transition of 2-Inverter Gate Where VBias = 25 mV**

Figure 1e shows the power Consumption for the test bench when a 25 mV bias voltage is applied. There is no significant difference in power consumption at this bias voltage compared to zero bias voltage.



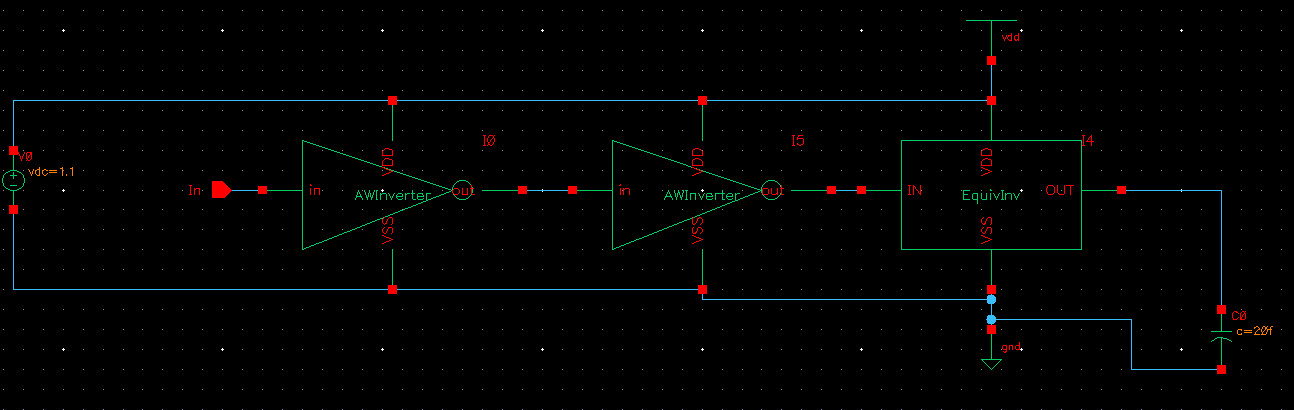
**Figure 1f: Total Power Consumption for Low-to-High Transition of 2-Inverter Gate Where VBias = 50 mV**

As we double the bias voltage, again we see very little change in power consumption. It appears to have a slightly lower maximum, but certainly not enough to begin to draw any conclusions.



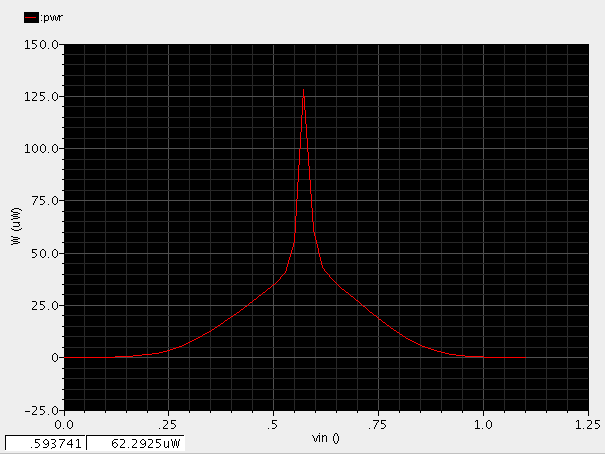
**Figure 1g: Total Power Consumption for Low-to-High Transition of 2-Inverter Gate Where VBias = 200 mV**

For the sake of the analysis, we increased the bias voltage to 200 mV in hopes to see a more concrete trend. This bias voltage is relatively high, but it gives us an exaggerated picture of how the power consumption is changing. Although the peak power consumption reduced by slightly more than 5 uW, we cannot draw any significant conclusions as to the total power consumption of the DelVGate during a high-low transition except that the power does not increase significantly with VBIAS.



**Figure 2a: Test Bench to Compare the High-Low Transition of an Equally Sized Inverter**

Figure 2a was designed to compare the power consumption of an inverter with the same logical effort to that of our DelVGate. Note that the load capacitance here is 20f F, which is equivalent to having two outputs tied to a 10f F load each.



**Figure 2b: Total Power Consumption of Equivalent Inverter During High-Low Transition**

Figure 2b illustrates what we hoped and expected, that the power consumption for a high-low transition of an equally sized inverter, given an equivalent load, was very close to that of our 2-inverter gate. Although we cannot conclude which gate (this inverter or our DelVGate) consumes more power during a high-low transition, it is important that we can illustrate that our new gate design does not consume significantly more power during a transition than an equally sized inverter.

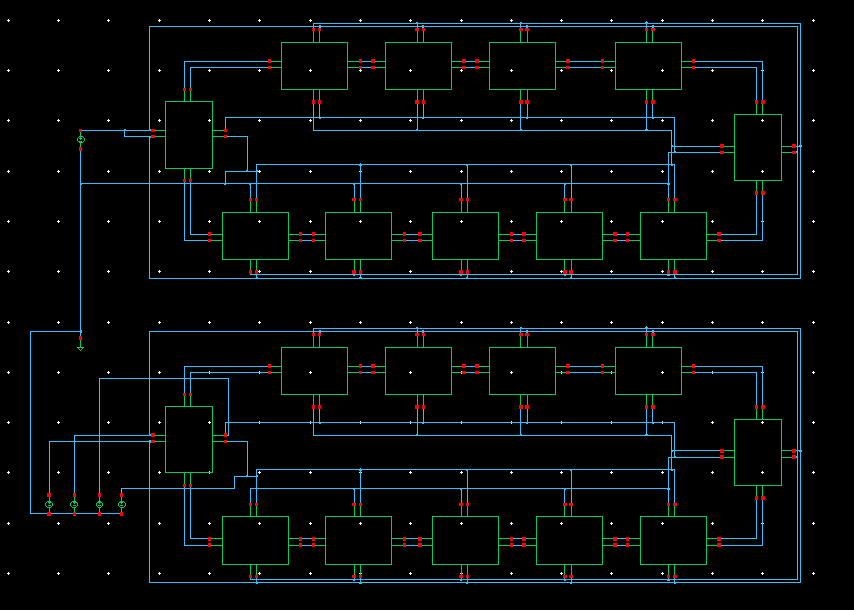
**Figure 3a: Two 11-Gate Ring Oscillators**

Figure 3a shows the test bench we used to evaluate how the frequency of a ring oscillator changes as we change the bias voltage. The top figure is the control oscillator, with no bias voltage. The bottom oscillator contains four voltage supplies so we can adjust VBIAS and interpret the results versus our control oscillator.

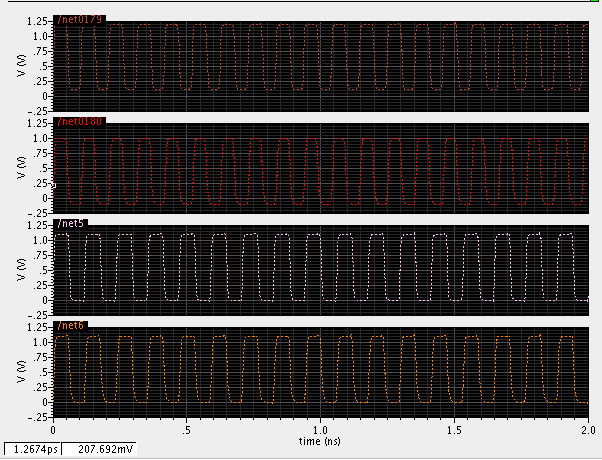


Figure 3b: Transient Response of Ring Oscillators

Figure 3b shows the transient responses of both ring oscillators. The control oscillator’s response is shown in the bottom two graphs, while the top two graphs show the response of the second oscillator with a bias voltage of 100mV. The reason that there are two graphs is that we wanted to evaluate both the high and low outputs of one gate in the ring oscillator. Refer to Figure 1a to see an illustration of what the high and low outputs for one gate are (denoted HiOut and LoOut ). It can be seen from these waveforms that the ring oscillator which incorporates a bias voltage has a higher frequency than the control oscillator.

**SUMMARIES**

*35 nm FinFETs*7

**Synopsis:** In [7], Fu-Liang, *et al.* depict what seems to be one of the very first operational FinFETs. They first present the 35 nm CMOS FinFET and then present findings from a simulated 10 nm CMOS FinFET. They use a standard doped n+ gate as well as a doped channel to regulate PMOS and NMOS threshold voltages. The authors explain that decreasing gate spacing reduces parasitic resistances and reducing fin thickness minimizes short channel effects, including DIBL. Table 1 shows that their 35 nm FinFET performs comparably to better than developments by other references and projected progress by IRTS and Fig. 6 shows hot carrier lifetime is much improved.

**Take-Aways:** Since MOSFETs are becoming more difficult to effectively scale, FinFETs were developed and proposed as a possible new direction for transistor technology. Both adaptive body biasing and FinFET technology seek to improve power consumption while enhancing or, at the very least, maintaining high frequency performance.

*Nanoscale FinFETs With Gate-Source/Drain Underlap*3

**Synopsis:** In [3], Trivedi, *et al.* simulate the behavior of FinFETs with G-S/D non-overlap, or underlap using the MEDICI model. The main focus of this paper is the effective channel length for optimal underlapped FinFET performance. The effective channel length bias is dependent on a “trade-off” between short channel effects and the S/D series resistance. The authors determine that G-S/D underlapping can, indeed, lead to optimal FinFET performance when the effective channel length is properly sized. The underlapping reduces G-S/D junction capacitances and maximizes G-G capacitance, which leads to increased CMOS drivability and speed and decreased S/D series resistance.

**Take-Aways:** Our takeaway from this paper is a more in-depth description of FinFETs and methods used for biasing dual-gate MOSFETs.

*Dynamic Sleep Transistor and Body Bias for Active Leakage Power Control of Microprocessors*4

**Synopsis:** In [3], Tschanz, *et al.* discuss a new technique for regulating leakage and switching power. They combine the techniques of adaptive body bias and clock gating with the addition of a “sleep transistor.” This sleep transistor is placed in series with the power supply. It is programmed to turn off when the chip enters standby, or idle mode, disconnecting the block from the power supply. The authors test a chip prototype implementing the aforementioned method and determine leakage and switching power are reduced with only slight consequences for performance. These results do, however, rely heavily on the block activity factor and number of clock cycles in idle mode. In general, the results of this technique will only improve with scaling, which makes it quite promising.

**Take-Aways:** This paper will be particularly helpful in our comparison between dynamic and static power consumption with increased bias voltage. It will also be helpful for determining how body biasing can be combined with other methods for maintaining (or, where possible, improving) performance while decreasing power dissipation in CMOS scaling.

*Effectiveness of Adaptive Supply Voltage and Body Bias for Reducing Impact of Parameter Variations in Low Power and High Performance Microprocessors6*

**Synopsis:** This paper discusses the advantages of adjusting the supply voltage to either increase the frequency or decrease the power usage to reduce the impact of die-to-die and within-die variations. Specifically, increasing the supply voltage increases both the frequency and power usage of a die, while decreasing the supply voltage does the opposite. Ultimately, adjusting the supply voltage adaptively results in more dies meeting their frequency and power consumption standards.

**Take-Aways:** The most important and relevant concept learned from this paper was that we can often realize the greatest reduction in power usage by adjusting supply voltages in paths other than the critical paths. This is because the overall frequency of the die is not greatly impacted when the frequencies of non-critical paths are reduced, and we can therefore achieve savings in power consumption at the cost of the frequency in non-critical paths. One thing to keep in mind when applying the technique is that it will usually result in more critical paths.

*Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers1*

**Synopsis:** This paper discusses the first ever FinFET manufactured on a Si wafer. It discusses the benefits of a FinFET, including its resistance to body biasing and short channel effects. This was an early publication on FinFETs, and it promotes them as a very promising technology as transistors are scaled smaller and smaller.

**Take-Aways:** Most relevant to our project is the fact that FinFETs are significantly more immune to body biasing effects than the MOSFETs used in most technologies today. This can reduce the effect of manufacturing variations, but will also hinder the designer’s ability to adjust the frequency and power usage of a die.

*NBTI Resilient Circuits Using Adaptive Body Biasing2*

**Synopsis:** This publication discusses reliability and lifetime of circuits and circuit components. It focuses on NBTI (Negative Bias Temperature Instability) of a PMOS transistor, and promotes a forward body biasing technique to reduce the impact NBTI has on a PMOS transistor. This paper also discusses methods for sending out signals before a catastrophic error occurs so a failing component can be repaired or replaced before the failure occurs.

**Take-Aways:** The most important concept to our project is how forward body biasing a PMOS transistor can reduce the impact of NBTI. This will prove to be an important consideration when determining the limitations of body biasing, and how body biasing affects the component’s lifetime.

*Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage5*

**Synopsis:** This paper discusses body biasing techniques to either reduce the power usage of a die that does not meet a power consumption requirement, or increasing the frequency of a die that does not meet a frequency requirement. Two methods are discussed: The first is a manual bias voltage applied to the body of a component that does not meet a certain specification by the designer. The second is an on-chip bias applied through a circuit design which evaluates frequency and power consumption and applies the bias voltages as needed. The on-chip design proved to maximize the frequency of a die given a power constraint, which resulted in more dies being accepted at higher frequencies.

**Take-Aways:** Most pertinent to our project is how forward and reverse body biasing affects the frequency and power consumption of a die. This paper gives great insight in adjusting body bias adaptively to compensate for parameter variations.

**REFERENCES**

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3. Trivedi, VP, et al. "Nanoscale FinFETs With Gate-Source/Drain Underlap." *IEEE Transactions on Electron Devices* 52.1 (2005): 56-62. *IEEE Xplore Digital Library*. 5 Oct. 2013.

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6. Tschanz, JW, S Narendra, R Nair, and V De. "Effectiveness of Adaptive Supply Voltage and Body bias for Reducing Impact of Parameter Variations in Low Power and High Performance Microprocessors." . Solid-State Circuits, IEEE Journal of, n.d. 21 September 2013.

7. Yang, F-L., et al. “35 nm CMOS FinFETs”, in *Symposium On VLSI Technology Digest of Technical Papers – Taiwan Semiconductor Manufacturing Company, Ltd.*, June 11-13, 2002, Honolulu, HI, 104-105.